CLAIMS

1. (previously presented) A programmable device comprising a Serial Peripheral Interface (SPI) adapted to be connected in parallel to an SPI interface of each of two or more SPI serial memory devices such that the programmable device is adapted to receive a different portion of configuration data stored in each SPI serial memory device without transmitting the configuration data via a controller connected between the SPI serial memory devices and the programmable device.

2. (previously presented) The invention of claim 1, wherein:
the programmable device is an FPGA; and
each SPI serial memory device is an SPI serial flash PROM.

3. (previously presented) The invention of claim 1, wherein the programmable device is adapted to independently generate at least one command adapted to control operations of each SPI serial memory device during configuration of the programmable device.

4. (previously presented) The invention of claim 1, wherein the programmable device is adapted to generate a message to inform each SPI serial memory device of a starting address to be used to transfer the configuration data stored in said each SPI serial memory device to the programmable device.

5. (previously presented) The invention of claim 1, wherein the programmable device is adapted to receive instructions to ignore data from at least one of the SPI serial memory devices.

6. (original) The invention of claim 5, wherein the programmable device is adapted to retrieve the instructions from the configuration data.

7. (canceled)

8. (previously presented) The invention of claim 1, wherein the programmable device is adapted to be instructed, based on information contained in the configuration data, as to how to interpret the different portions of the configuration data received from the different SPI serial memory devices.

9. (previously presented) The invention of claim 1, wherein the programmable device is adapted to process different amounts of configuration data received from different SPI serial memory devices.

10. (original) The invention of claim 9, wherein the two or more different SPI serial memory devices are of two or more different sizes capable of storing the different amounts of the configuration data.

11. (original) The invention of claim 9, wherein the programmable device is adapted to stop including data from an SPI serial memory device that has already transmitted all of its configuration data.

12. (previously presented) The invention of claim 1, wherein the programmable device comprises:
a multiplexer (mux) adapted to interleave the configuration data from the two or more different SPI serial memory devices; and

a timing controller adapted to control the operations of the mux and to generate a configuration clock signal used to control the timing of the reading of the configuration data from the two or more different SPI serial memory devices.

13. (original) The invention of claim 12, wherein the timing controller is adapted to (1) change the operations of the mux and (2) change the rate of the configuration clock signal, when the number of SPI serial memory devices having configuration data to transmit changes.

14. (previously presented) The invention of claim 1, wherein each different portion of the configuration data from the corresponding SPI serial memory device is received at a different configuration data input pin of the SPI interface of the programmable device.

15. (previously presented) The invention of claim 1, wherein each of one or more output pins of the programmable device is adapted to be connected to corresponding pins of all of the SPI serial memory devices.

16. (original) The invention of claim 15, wherein the programmable device has a configuration clock signal pin adapted to be connected to corresponding configuration clock signal pins of all of the SPI serial memory devices such that configuration data is transmitted simultaneously from all of the SPI serial memory devices to the programmable device.

17. (previously presented) An apparatus comprising:
a programmable device having a Serial Peripheral Interface (SPI); and
two or more SPI serial memory devices, each having an SPI interface, wherein:
the SPI interface of the programmable device is connected in parallel to the SPI interfaces of the SPI serial memory devices such that the programmable device is adapted to receive a different portion of configuration data stored in each different SPI serial memory device without transmitting the configuration data via a controller connected between the SPI serial memory devices and the programmable device.

18. (previously presented) A method for configuring a programmable device, comprising:
reading a different portion of configuration data from a Serial Peripheral Interface (SPI) of each of two or more different SPI serial memory devices connected in parallel to an SPI interface of the programmable device without transmitting the configuration data via a controller connected between the SPI serial memory devices and the programmable device; and
configuring the programmable device using the configuration data.

19. (currently amended) A programmable device adapted to be connected in parallel to two or more memory devices such that the programmable device is adapted to receive configuration data stored in the two or more memory devices without transmitting the configuration data via a controller connected between any of the memory devices and the programmable device, wherein the programmable device is adapted to receive a different portion of the configuration data from each different memory device, and wherein one or more of (a)-(i):
(a) the programmable device has an SPI interface;
each memory device is an SPI serial memory device having an SPI interface; and
the SPI interface of each SPI serial memory device is connected to the SPI interface of the programmable device;
(b) the programmable device is adapted to independently generate at least one command adapted to control operations of the memory devices during configuration of the programmable device;

(c) the programmable device is adapted to generate a message to inform the memory devices of a starting address to be used to transfer the configuration data stored in the memory devices to the programmable device;

(d) the programmable device is adapted to receive instructions to ignore data from a memory device;

(e) the programmable device is adapted to be instructed, based on information contained in the configuration data, as to how to interpret the different portions of the configuration data received from the different memory devices;

(f) the programmable device is adapted to process different amounts of configuration data received from different memory devices;

(g) the programmable device comprises:

a multiplexer (mux) adapted to interleave the configuration data from the two or more different memory devices; and

a timing controller adapted to control the operations of the mux and to generate a configuration clock signal used to control the timing of the reading of the configuration data from the two or more different memory devices;

(h) each different portion of the configuration data from the corresponding memory device is received at a different configuration data input pin of the programmable device; and

(i) each of one or more output pins of the programmable device is adapted to be connected to corresponding pins of all of the memory devices; and

the programmable device has a configuration clock signal pin adapted to be connected to corresponding configuration clock signal pins of all of the memory devices such that configuration data is transmitted simultaneously from all of the memory devices to the programmable device.

20. (original) The invention of claim 19, wherein:

the programmable device has an SPI interface;

each memory device is an SPI serial memory device having an SPI interface; and

the SPI interface of each SPI serial memory device is connected to the SPI interface of the programmable device.

21. (currently amended) The invention of claim 19, wherein the programmable device is adapted to independently generate the at least one command adapted to control the operations of the memory devices during the configuration of the programmable device.

22. (currently amended) The invention of claim 19, wherein the programmable device is adapted to generate [[a]] the message to inform the memory devices of [[a]] the starting address to be used to transfer the configuration data stored in the memory devices to the programmable device.

23. (currently amended) The invention of claim 19, wherein the programmable device is adapted to receive the instructions to ignore the data from [[a]] the memory device.

24. (original) The invention of claim 23, wherein the programmable device is adapted to retrieve the instructions from the configuration data.

25. (currently amended) The invention of claim 19, wherein the programmable device is adapted to be instructed, based on the information contained in the configuration data, as to how to interpret the different portions of the configuration data received from the different memory devices.

26. (currently amended) The invention of claim 19, wherein the programmable device is adapted to process the different amounts of configuration data received from the different memory devices.

27. (original) The invention of claim 26, wherein the two or more different memory devices are of two or more different sizes capable of storing the different amounts of the configuration data.

28. (original) The invention of claim 26, wherein the programmable device is adapted to stop including data from a memory device that has already transmitted all of its configuration data.

29. (currently amended) The invention of claim 19, wherein the programmable device comprises:

[[a]] the multiplexer (mux) adapted to interleave the configuration data from the two or more different memory devices; and

[[a]] the timing controller adapted to control the operations of the mux and to generate [[a]] the configuration clock signal used to control the timing of the reading of the configuration data from the two or more different memory devices.

30. (original) The invention of claim 29, wherein the timing controller is adapted to (1) change the operations of the mux and (2) change the rate of the configuration clock signal, when the number of memory devices having configuration data to transmit changes.

31. (original) The invention of claim 19, wherein each different portion of the configuration data from the corresponding memory device is received at a different configuration data input pin of the programmable device.

32. (currently amended) The invention of claim 19, wherein each of one or more output pins of the programmable device is adapted to be connected to corresponding pins of all of the memory devices, wherein the programmable device has the configuration clock signal pin adapted to be connected to the corresponding configuration clock signal pins of all of the memory devices such that the configuration data is transmitted simultaneously from all of the memory devices to the programmable device.

33. (canceled)

34. (currently amended) An apparatus comprising:

a programmable device; and

two or more memory devices, wherein:

the programmable device is connected in parallel to each memory device such that the programmable device is adapted to receive configuration data stored in the two or more memory devices without transmitting the configuration data via a controller connected between any of the memory devices and the programmable device, wherein the programmable device is adapted to receive a different portion of the configuration data from each different memory device, and wherein one or more of (a)-(i):

(a) the programmable device has an SPI interface;

each memory device is an SPI serial memory device having an SPI interface; and

the SPI interface of each SPI serial memory device is connected to the SPI interface of the programmable device;

(b) the programmable device is adapted to independently generate at least one command adapted to control operations of the memory devices during configuration of the programmable device;

(c) the programmable device is adapted to generate a message to inform the memory devices of a starting address to be used to transfer the configuration data stored in the memory devices to the programmable device;

(d) the programmable device is adapted to receive instructions to ignore data from a memory device;

(e) the programmable device is adapted to be instructed, based on information contained in the configuration data, as to how to interpret the different portions of the configuration data received from the different memory devices;

(f) the programmable device is adapted to process different amounts of configuration data received from different memory devices;

(g) the programmable device comprises:

a multiplexer (mux) adapted to interleave the configuration data from the two or more different memory devices; and

a timing controller adapted to control the operations of the mux and to generate a configuration clock signal used to control the timing of the reading of the configuration data from the two or more different memory devices;

(h) each different portion of the configuration data from the corresponding memory device is received at a different configuration data input pin of the programmable device; and

(i) each of one or more output pins of the programmable device is adapted to be connected to corresponding pins of all of the memory devices; and

the programmable device has a configuration clock signal pin adapted to be connected to corresponding configuration clock signal pins of all of the memory devices such that configuration data is transmitted simultaneously from all of the memory devices to the programmable device.

35. (currently amended) A method for configuring a programmable device, comprising:

simultaneously reading configuration data from two or more memory devices connected in parallel to the programmable device without transmitting the configuration data via a controller connected between any of the memory devices and the programmable device, wherein the programmable device receives a different portion of the configuration data from each different memory device; and

configuring the programmable device using the configuration data, wherein one or more of (a)-(i):

(a) the programmable device has an SPI interface;

each memory device is an SPI serial memory device having an SPI interface; and

the SPI interface of each SPI serial memory device is connected to the SPI interface of the programmable device;

(b) the programmable device is adapted to independently generate at least one command adapted to control operations of the memory devices during configuration of the programmable device;

(c) the programmable device is adapted to generate a message to inform the memory devices of a starting address to be used to transfer the configuration data stored in the memory devices to the programmable device;

(d) the programmable device is adapted to receive instructions to ignore data from a memory device;

(e) the programmable device is adapted to be instructed, based on information contained in the configuration data, as to how to interpret the different portions of the configuration data received from the different memory devices;

(f) the programmable device is adapted to process different amounts of configuration data received from different memory devices;

(g) the programmable device comprises:

a multiplexer (mux) adapted to interleave the configuration data from the two or more different memory devices; and

a timing controller adapted to control the operations of the mux and to generate a configuration clock signal used to control the timing of the reading of the configuration data from the two or more different memory devices;

(h) each different portion of the configuration data from the corresponding memory device is received at a different configuration data input pin of the programmable device; and

(i) each of one or more output pins of the programmable device is adapted to be connected to corresponding pins of all of the memory devices; and

the programmable device has a configuration clock signal pin adapted to be connected to corresponding configuration clock signal pins of all of the memory devices such that configuration data is transmitted simultaneously from all of the memory devices to the programmable device.

36. (previously presented) The invention of claim 1, wherein the different portions of the configuration data are adapted to be simultaneously transmitted in parallel to the programmable device.

37. (previously presented) The invention of claim 17, wherein the different portions of the configuration data are adapted to be simultaneously transmitted in parallel to the programmable device.

38. (previously presented) The invention of claim 18, wherein the different portions of the configuration data are simultaneously transmitted in parallel to the programmable device.

39. (previously presented) The invention of claim 19, wherein the different portions of the configuration data are adapted to be simultaneously transmitted in parallel to the programmable device.

40. (previously presented) The invention of claim 34, wherein the different portions of the configuration data are adapted to be simultaneously transmitted in parallel to the programmable device.

41. (previously presented) A programmable device comprising a Serial Peripheral Interface (SPI) adapted to be connected to an SPI interface of at least one SPI serial memory device such that the programmable device is adapted to receive configuration data stored in the SPI serial memory device without transmitting the configuration data via a controller connected between the SPI serial memory device and the programmable device, wherein the programmable device is adapted to receive instructions to ignore data from an SPI serial memory device.

42. (previously presented) The invention of claim 41, wherein the programmable device is adapted to retrieve the instructions from the configuration data.